Using a Multiple Voltage Supervisor for Over and Under Voltage Power Supply Shutdown and Fault Monitoring

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Author: Carlos Martinez

Introduction

Reliable system operation is often dependent on the quality of the power supplied. Supply voltages that are too low can cause faulty operation as the microcontroller, FPGA, or ASIC begins to send bad data to memories or peripheral devices. A voltage that is too high can permanently damage system components. So, it is often necessary to add protection circuits to the design. In addition to providing protection in the event of a voltage fluctuation, it is also valuable to identify the source of a failure.

This application uses an X40435 device from Intersil along with 2 FETs and some resistors to provide power shutoff. The 2-wire interface and fault register of the X40435 provides fault monitoring capability. This device also includes 4kbits of EEPROM for maintaining information, such as manufacturing and service records.

The X40435-C monitors three input voltages with voltage thresholds of 4.6V, 2.9V, and 1.0V. The circuit of Figure 4 shows a circuit that turns off the 3.3V output if a 5V supply is too low, or if the 3.3V supply is too low or too high.

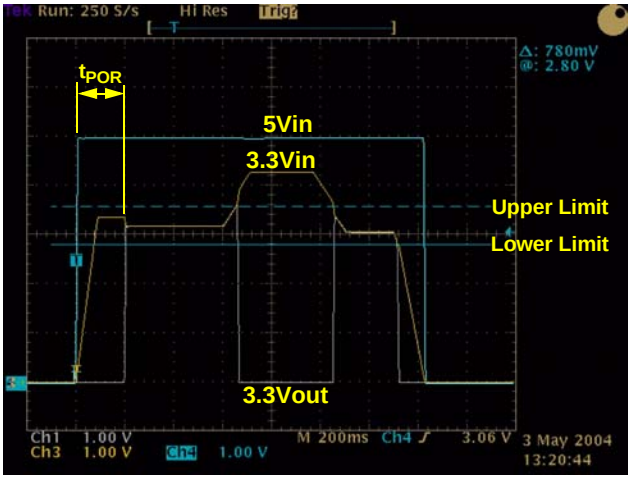
A Siliconix Si3443 MOSFET is used as the primary pass element (switch). This is a PMOS device that requires a V_{GS} of only 2.5V to turn on with an R_{DSon} of less than 0.1Ω so it can be used on power supplies down to 2.5V. The gate of this FET is controlled by the X40435 through a 2N7002 FET (which has a minimum V_{GS} of 2.5V). See Figure 4. For lower voltages, both the Si3443 and the 2N7002 could be replaced by a dual MOSFET, such as the Si4913, which has a V_{GS} of 1.8V and RDSon (at 1.8V) of 24mΩ.

The VCC input monitor of the X40435 turns off its open drain $\overline{\text{RESET}}$ output 200ms (t_{POR}) after VCC goes above the threshold of 4.6V. The V3MON input monitor of the X40435 turns off its open drain $\overline{\text{V3FAIL}}$ output when the 3.3V supply goes above 2.9V. When both of these conditions are valid, the gate of the 2N7002 is pulled high and turns on, allowing the $\overline{\text{V2FAIL}}$ output to control the gate of the Si3443. Note: if the tPOR time delay is not desired on the 5V input, then the $\overline{\text{LOWLINE}}$ output can replace the $\overline{\text{RESET}}$ output.

The V2MON input of the X40435 receives a voltage divided down from the 3.3V supply. The resistor divider is set such that the V2MON voltage is 1V when the 3.3V supply reaches 3.6V (the overvoltage level.) When the 3.3V is below 3.6V, the $\overline{\text{V2FAIL}}$ output is LOW. This turns on the Si3443 MOSFET, which supplies power to the load.

When the 3.3V supply reaches 3.6V, the $\overline{\text{V2FAIL}}$ output goes HIGH, turning off the output supply. When either the 3.3V or 5V supplies drops below their respective thresholds, the 2N7002 device turns off and the gate of the Si3443 is pulled HIGH, again turning off the load. Figure 1 shows the response of the circuit.

Figure 1. OV/UV Shutdown



The X40435 has a 2-wire interface that allows access to the EEPROM and the Fault Detection Register (see Figure 2). When the X40435 powers up, it resets all fault bits to zero. Also, any fault condition causes the related bit to reset to zero. Therefore, if the microcontroller checks the fault bits first, before writing them all to ones, it can determine what caused the system reset. If, for example, all bits are zero, then the 5V input supply powered off. If the LV3F bit is zero, then there was a 3.3V dropout. If the LV2F bit is zero, then the V2MON supply went above its threshold, then dropped back below it — indicating an overvoltage condition. There are also bits to indicate a Watchdog timer time-out or a manual reset of the system.

Figure 2. X40435 Fault Register

LV1F	LV2F	LV3F	WDF	MRF	0	0	0

A variation of this circuit is shown in Figure 5. In this circuit, an undervoltage condition on the 3.3V supply or 5V supply causes the system to be reset. That is, the 3.3V supply is not cut off. The 3.3V supply is turned off to the load only when the 3.3V input exceeds the maximum limit.

Figure 3. OV Shutdown/UV Reset

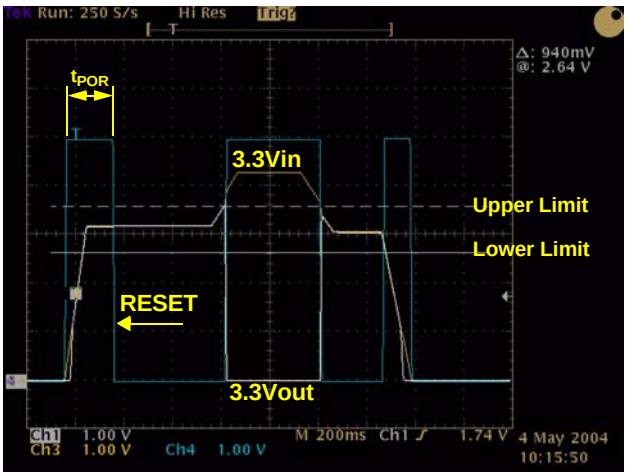


Figure 4. Basic OV Shutdown/UV Circuit

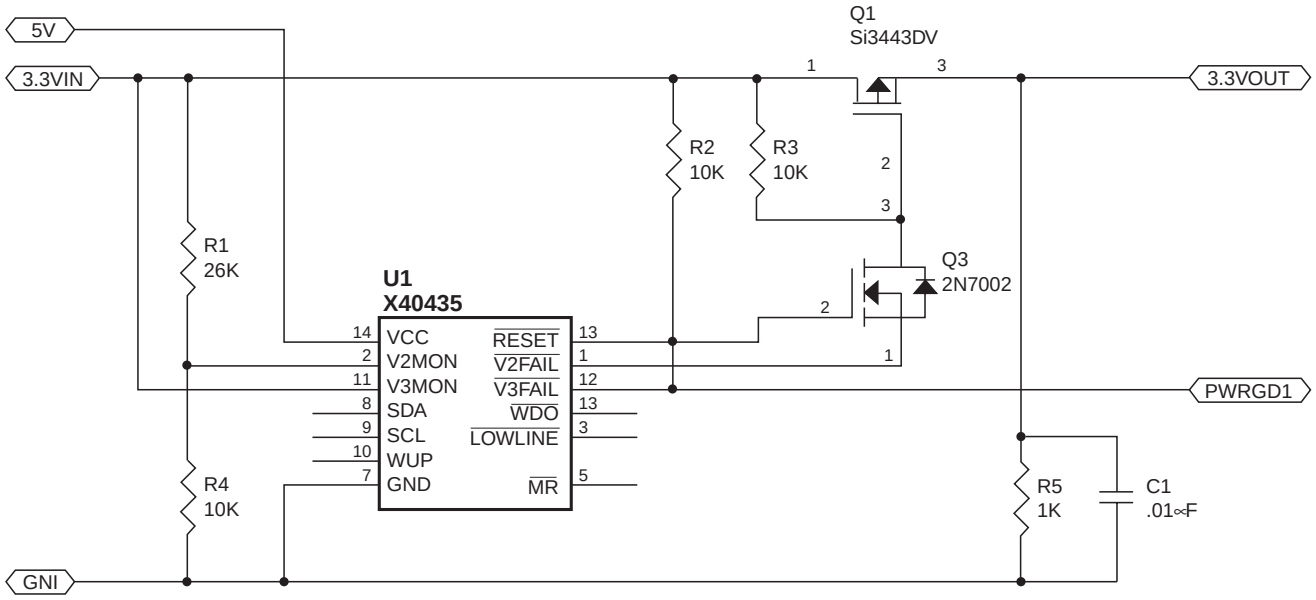


Figure 5. OV Shutdown/UV Reset Circuit